Weiss Engineering Ltd. OP1-BP

Features

Noise

$1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ voltage noise density at 1 kHz
$30\,\mathrm{nV_{PP}}$ voltage noise 0.1–10 Hz
$0.7\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ current noise density at 1 kHz
$80\,\mathrm{pA_{PP}}$ current noise 0.1–10 Hz

THD+N

−152 dB (+20 dBu, 1 kHz, 22 kHz BW, 600 Ω load)
−148 dB (+20 dBu, 10 kHz, 80 kHz BW, 600 Ω load)

AC characteristics

$50\,\mathrm{V}/\mu\mathrm{s}$ slew-rate, highly symmetrical
95 MHz gain bandwidth (G = 80 dB)
700 kHz full power bandwidth ($20\,\mathrm{V_{PP}}$ into 600 Ω)
300 kHz full power bandwidth ($20\,\mathrm{V_{PP}}$ into 200 Ω)

DC characteristics

$\pm10\,\mu\mathrm{V}$ input offset voltage
±60 nA input bias current
±2 nA input offset current

Load driving capability

$27\,\mathrm{V_{PP}}$ (+21.8 dBu) into 200 Ω (±15 V supply)
$20\,\mathrm{V_{PP}}$ (+19.2 dBu) into 100 Ω (±15 V supply)
$10\,\mathrm{V_{PP}}$ (+13.2 dBu) into 50 Ω (±15 V supply)
adjustable class A output current

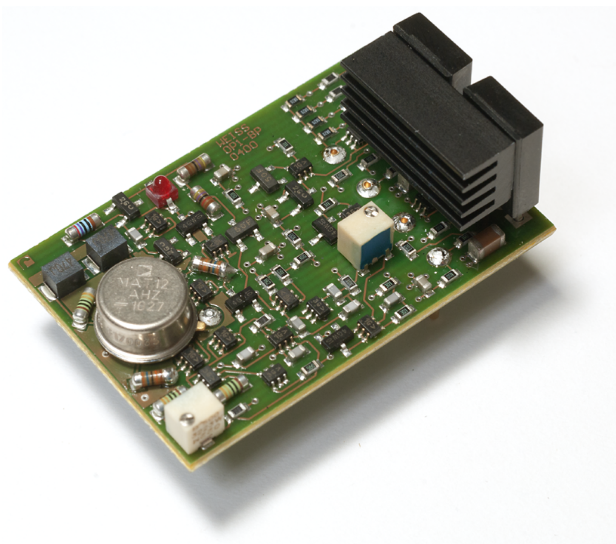
Applications

- high performance audio
- low noise, low distortion preamplifiers
- high resolution ADC drivers
- high resolution DAC IV converters
- headphone amplifiers and high-power line driver
- low distortion active filters
- high resolution instrumentation

General Description

The OP1-BP is a discrete operational amplifier particularly optimised for audio applications. Its wide output swing and superior load driving capability ($27\,\mathrm{V_{PP}}$ into 200 Ω), very low distortion (−152 dB) and very low noise ($1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$) leads to signal paths with exceptionally wide dynamic range. The excellent AC characteristics ($50\,\mathrm{V}/\mu\mathrm{s}$ slew-rate and 95 MHz gain bandwidth) ensures exemplary performance at ultrasound frequencies. This is combined with low input offset voltage ($\pm10\,\mu\mathrm{V}$), low input bias and input offset current (±60 nA and ±10 nA), good CMRR and PSRR (130 dB) and wide power supply range (±5 V to ±18 V) to form a true high performance general purpose amplifier.

Besides high-end audio the OP1-BP is useful for any critical application which requires very wide dynamic range and low distortion analogue signal processing; typical examples include spectrum analyzers, infrared detectors and low distortion oscillators.



Contents

Chapter 1

Revision History

2011-10-27, Revision 2: Revision history section added; typical performance characteristics section extended; outline dimensions section extended.

2011-01-21, Revision 1: Initial revision, preliminary.

Chapter 2

Specifications

The following specifications apply for $T_A = +25°$ C, $V_S = \pm 15$ V and amplifier fully warmed up unless otherwise noted.

Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage			±10	±50	μV
Input Offset Current			±2		nA
Input Bias Current			±60	±150	nA
Open Loop Gain	$R_L = 600\,\Omega$		136		dB
	$R_L = 200\,\Omega$		134		dB
Gain Bandwidth Product	G = 80 dB		95		MHz
Unity Gain Frequency			8		MHz
Slew Rate	$R_L = 600\,\Omega$		±50		V/μs
Power Supply Rejection	f = 10 Hz		130		dB
Input Voltage Noise Density	f = 1 kHz		1		$nV/\sqrt{Hz}$
	f = 10 Hz		1		$nV/\sqrt{Hz}$
Input Voltage Noise	0.1–10 Hz		30		nV_{PP}
Input Voltage Noise Density 1/f Corner			0.6		Hz
Input Current Noise Density	f = 1 kHz		0.7		$pA/\sqrt{Hz}$
	f = 10 Hz		1.4		$pA/\sqrt{Hz}$
Input Current Noise	0.1–10 Hz		80		pA_{PP}
Input Current Noise Density 1/f Corner			23		Hz
Output Voltage Swing	$R_L = 600\,\Omega$		±14		V
	$R_L = 200\,\Omega$		±13.5		V
	$R_L = 100\,\Omega$		±10		V
	$R_L = 50\,\Omega$		±5		V
Factory Preset Class A Output Current			±30		mA
Recommended Power Supply Voltage		±5		±18	V
Quiescent Current	no load		42		mA
Ground Pin Current			6.5		μA

Chapter 3

Absolute Maximum Ratings

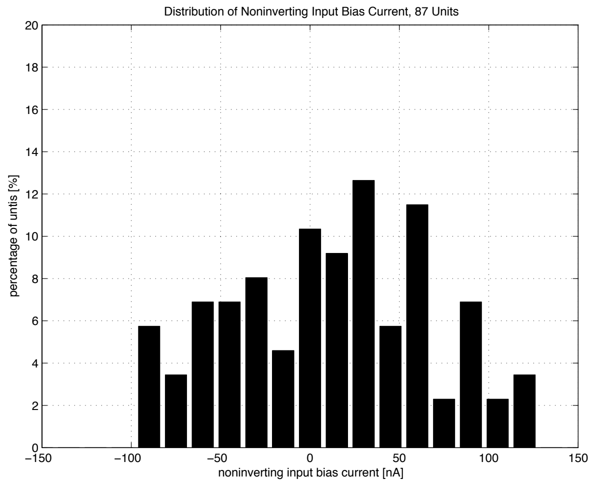
Parameter	**Ratings**
Supply Voltage	±22 V
Input Voltage	VCC + 0.7 V
	VEE − 0.7 V
Differential Input Current	±100 mA
Maximum Power Dissipation	3 W
Output Short-Circuit Duration	Indefinite Within Maximum Power Dissipation
Storage Temperature Range	−65° C to +125° C
Operating Temperature Range	−40° C to +85° C
Lead Temperature (Soldering, 10 sec.)	300° C

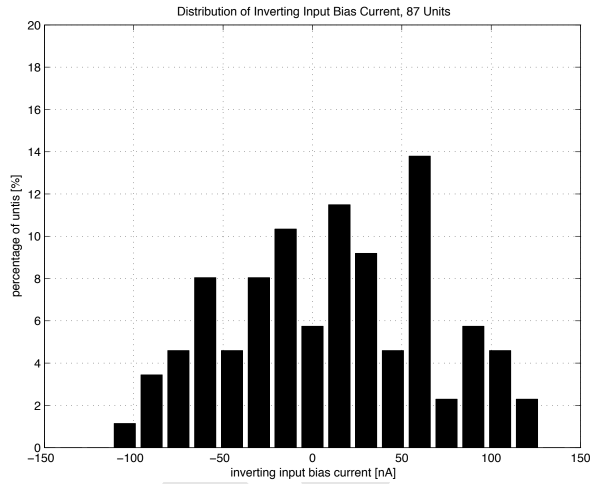
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

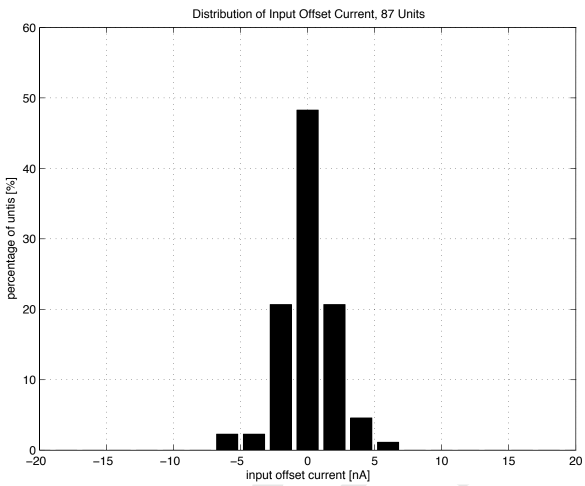
Chapter 4

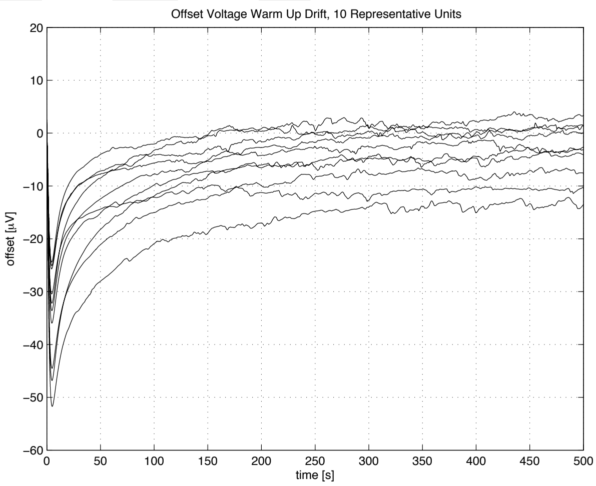
Typical Performance Characteristics

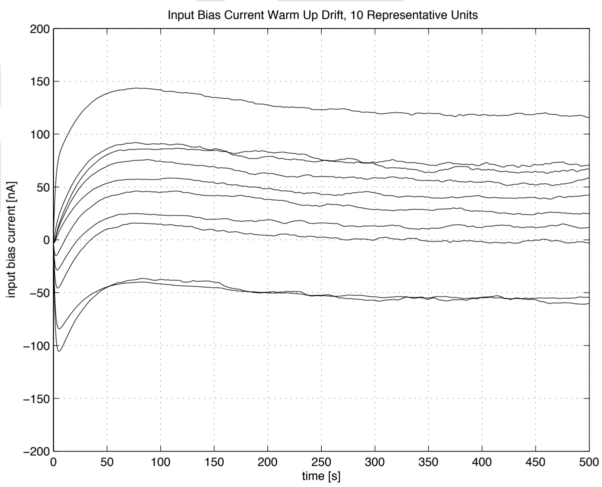
The following typical performance characteristics apply for $T_A = +25°$ C, $V_S = \pm 15$ V and the amplifier fully warmed up unless otherwise noted.

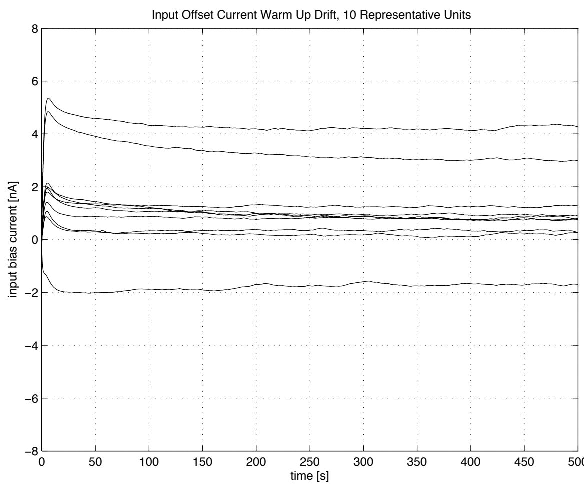

Distribution of Noninverting Input Bias Current, 87 Units
percentage of untis [%]
noninverting input bias current [nA]

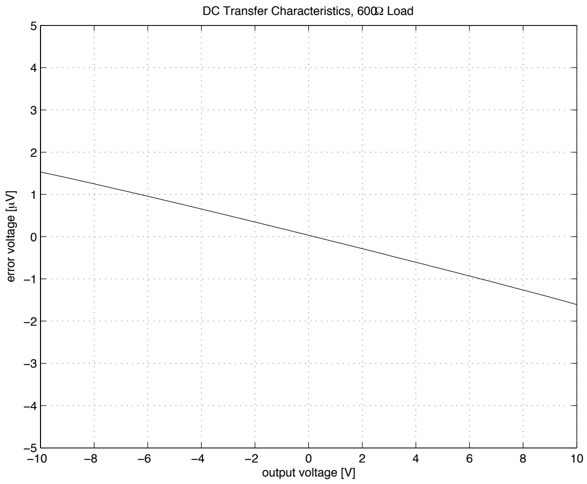

Distribution of Inverting Input Bias Current, 87 Units
percentage of untis [%]
inverting input bias current [nA]

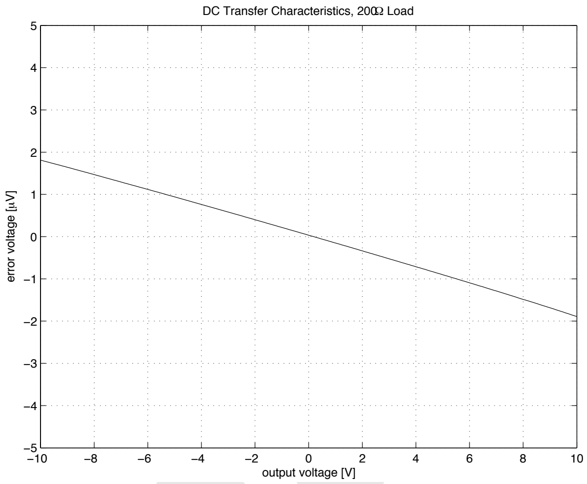

Distribution of Input Offset Current, 87 Units
percentage of untis [%]
input offset current [nA]

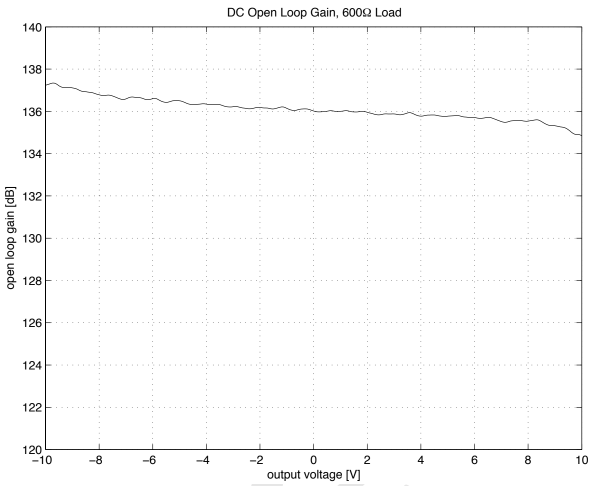

Offset Voltage Warm Up Drift, 10 Representative Units
offset [µV]
time [s]

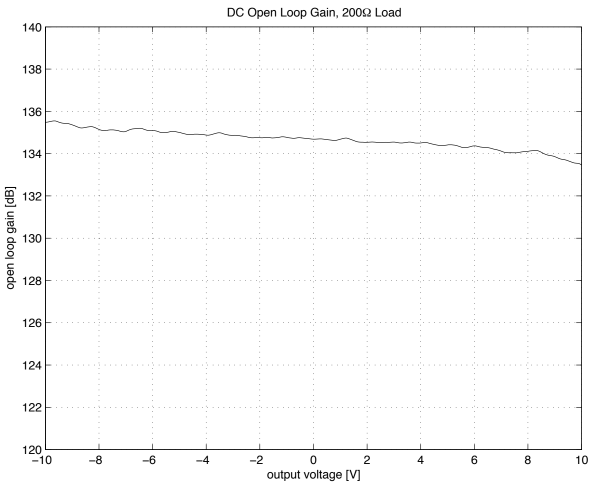

Input Bias Current Warm Up Drift, 10 Representative Units
input bias current [nA]
time [s]

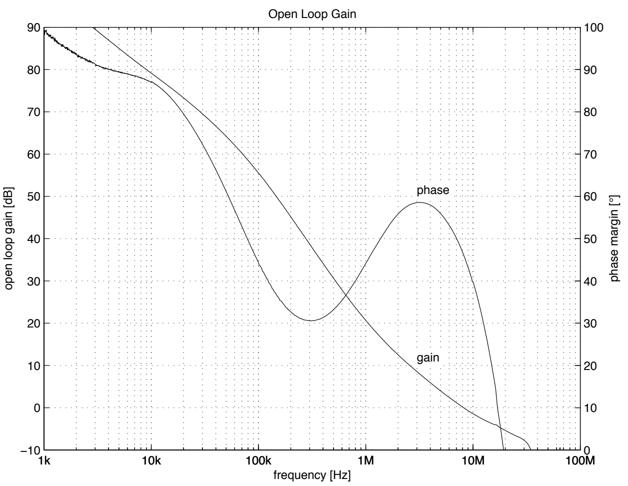

Input Offset Current Warm Up Drift, 10 Representative Units
input bias current [nA]
time [s]

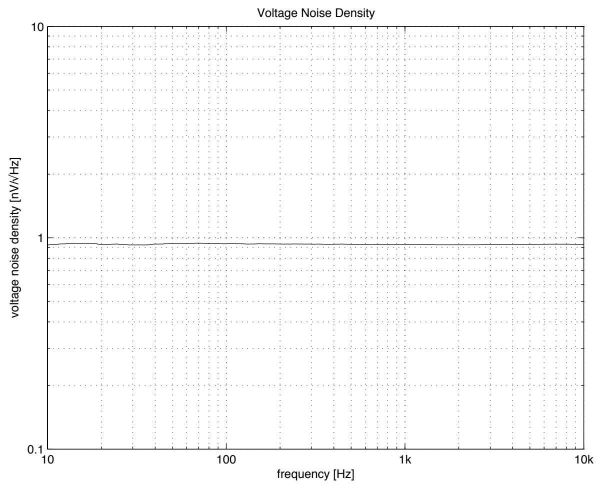

DC Transfer Characteristics, 600Ω Load
error voltage [μV]
output voltage [V]

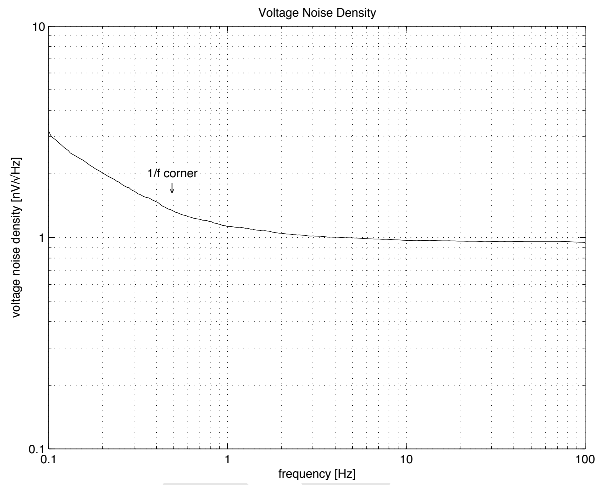

DC Transfer Characteristics, 200Ω Load
error voltage [μV]
output voltage [V]

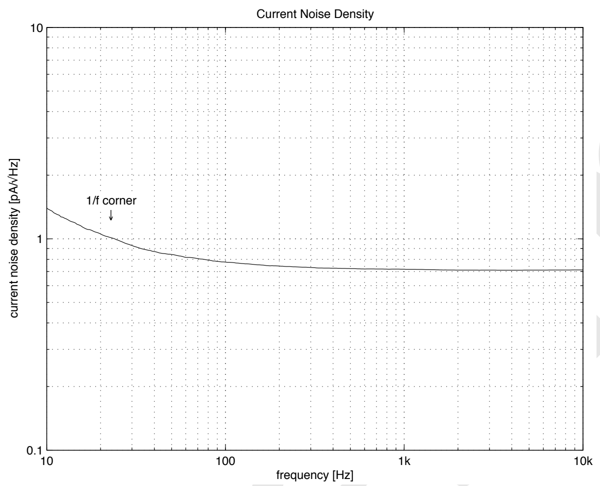

DC Open Loop Gain, 600Ω Load
open loop gain [dB]
output voltage [V]

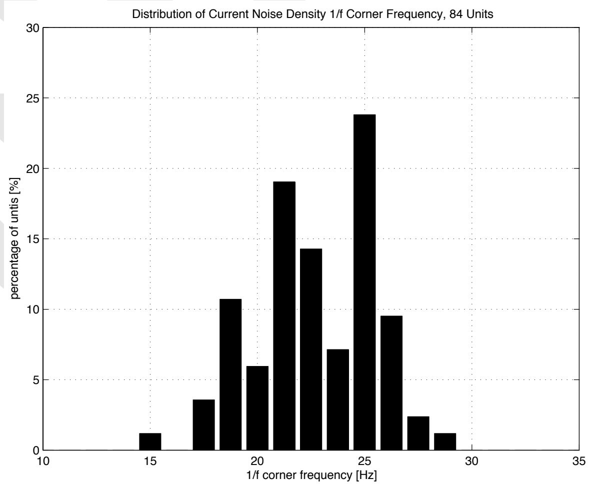

DC Open Loop Gain, 200Ω Load
open loop gain [dB]
output voltage [V]

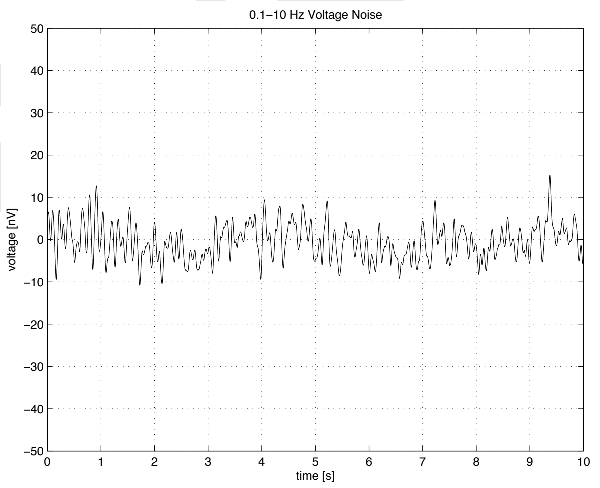

Open Loop Gain
open loop gain [dB]
phase margin [°]
frequency [Hz]
phase
gain

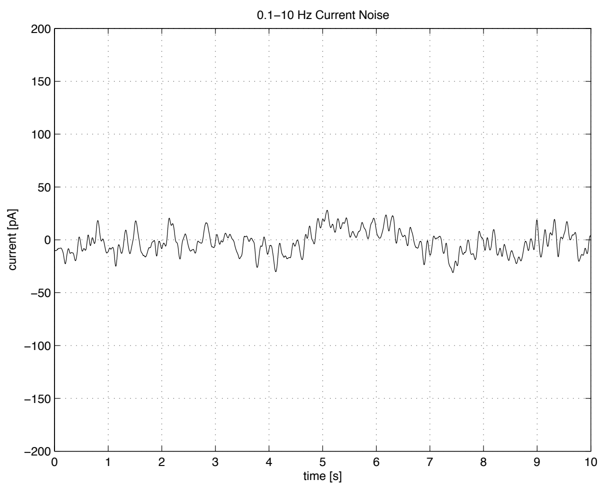

Voltage Noise Density
voltage noise density [nV/√Hz]
frequency [Hz]

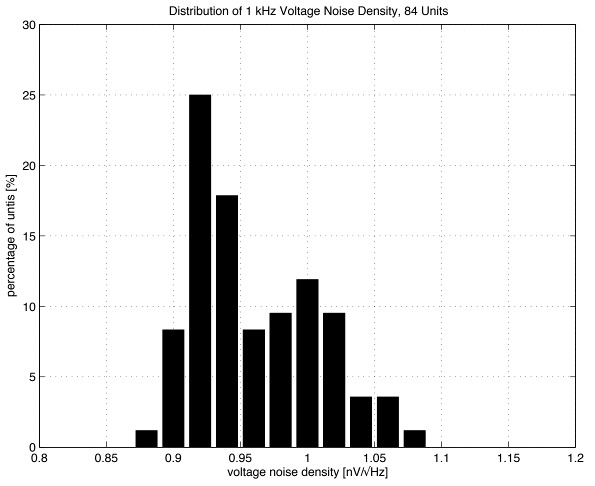

Voltage Noise Density
1/f corner
voltage noise density [nV/√Hz]
frequency [Hz]

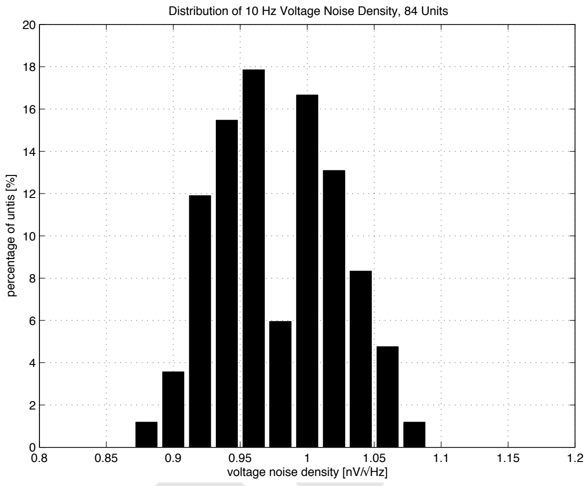

Current Noise Density
1/f corner
current noise density [pA/√Hz]
frequency [Hz]

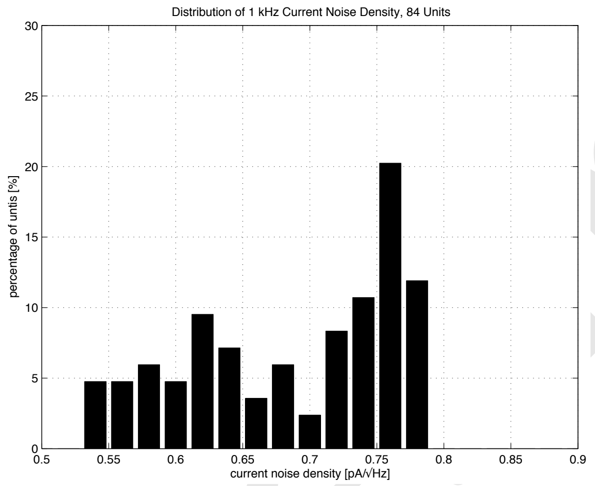

Distribution of Current Noise Density 1/f Corner Frequency, 84 Units
percentage of untis [%]
1/f corner frequency [Hz]

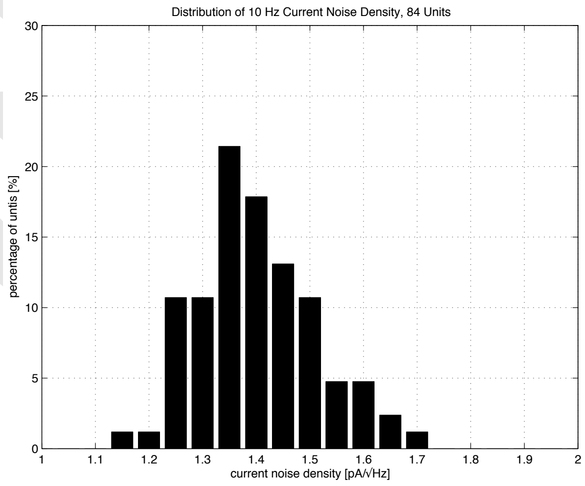

0.1−10 Hz Voltage Noise
voltage [nV]
time [s]

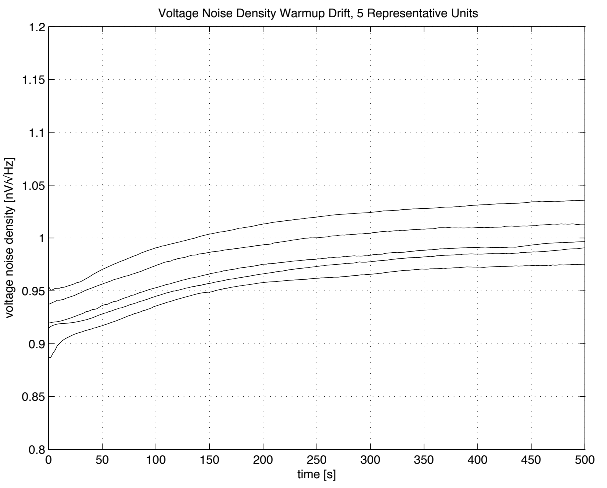

0.1−10 Hz Current Noise
current [pA]
time [s]

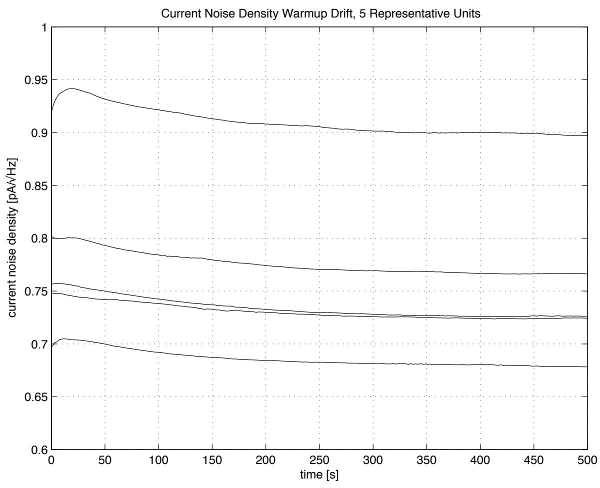

Distribution of 1 kHz Voltage Noise Density, 84 Units
percentage of untis [%]
voltage noise density [nV/√Hz]

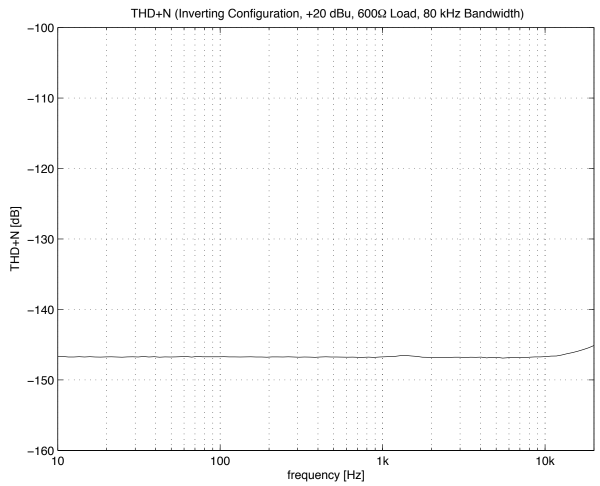

Distribution of 10 Hz Voltage Noise Density, 84 Units
percentage of untis [%]
voltage noise density [nV/√Hz]

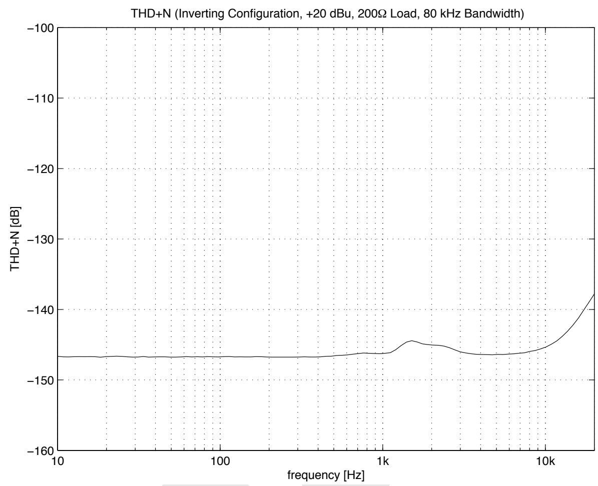

Distribution of 1 kHz Current Noise Density, 84 Units
percentage of untis [%]
current noise density [pA/√Hz]

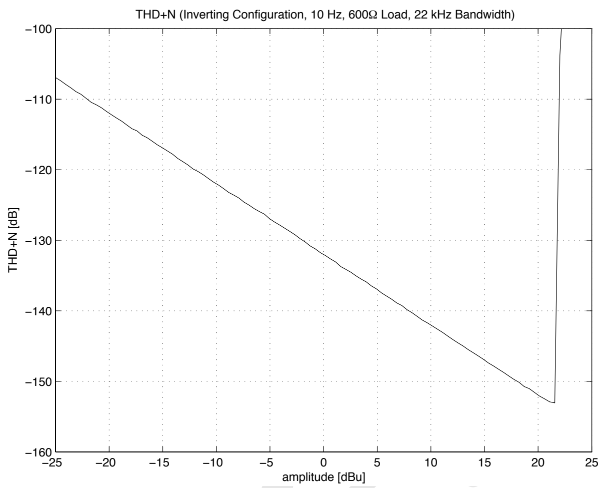

Distribution of 10 Hz Current Noise Density, 84 Units
percentage of untis [%]
current noise density [pA/√Hz]

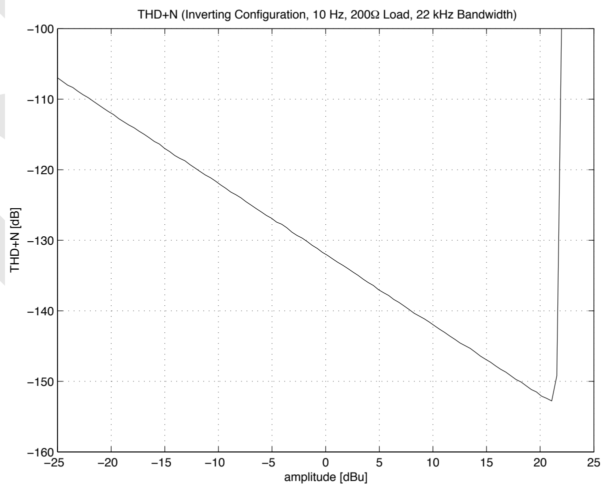

Voltage Noise Density Warmup Drift, 5 Representative Units
voltage noise density [nV/√Hz]
time [s]

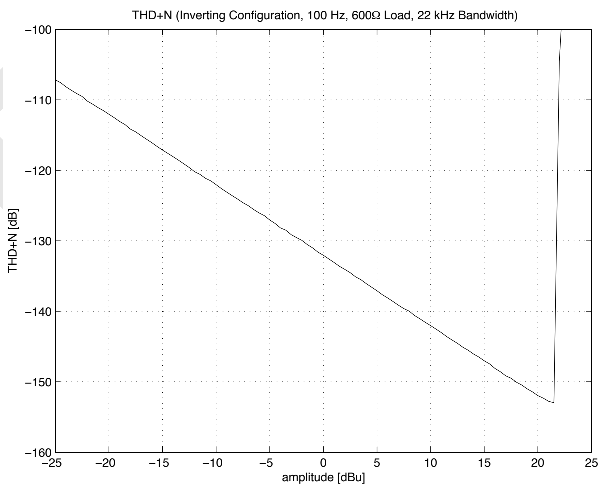

Current Noise Density Warmup Drift, 5 Representative Units
current noise density [pA/√Hz]
time [s]

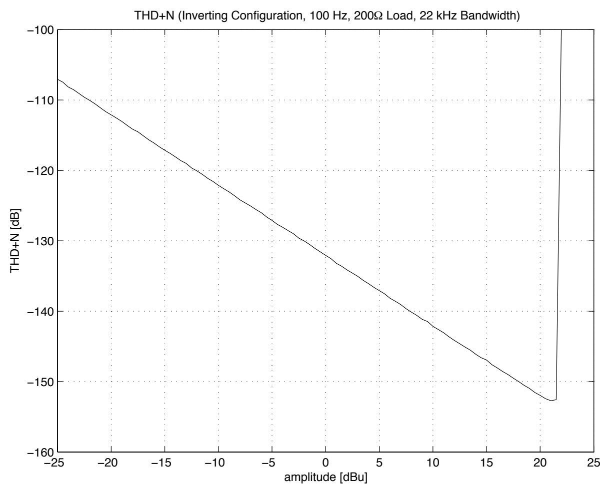

THD+N (Inverting Configuration, +20 dBu, 600Ω Load, 80 kHz Bandwidth)
THD+N [dB]
frequency [Hz]

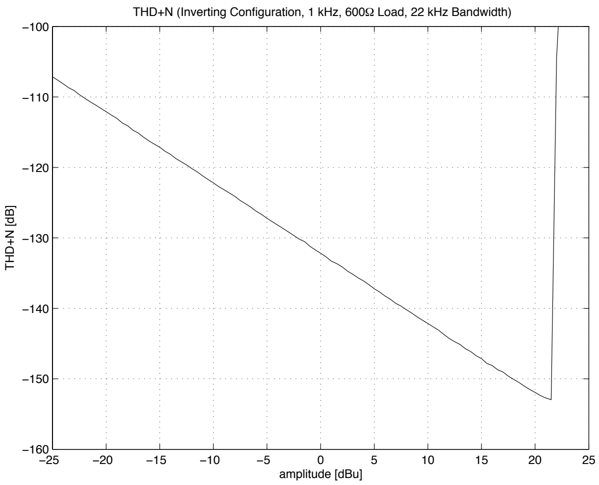

THD+N (Inverting Configuration, +20 dBu, 200Ω Load, 80 kHz Bandwidth)
THD+N [dB]
frequency [Hz]

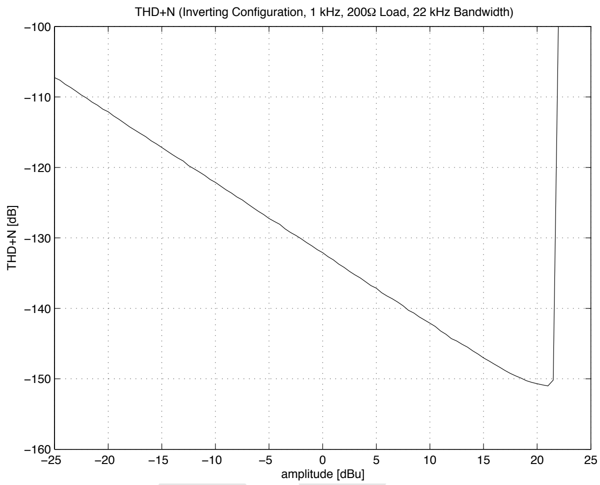

THD+N (Inverting Configuration, 10 Hz, 600Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

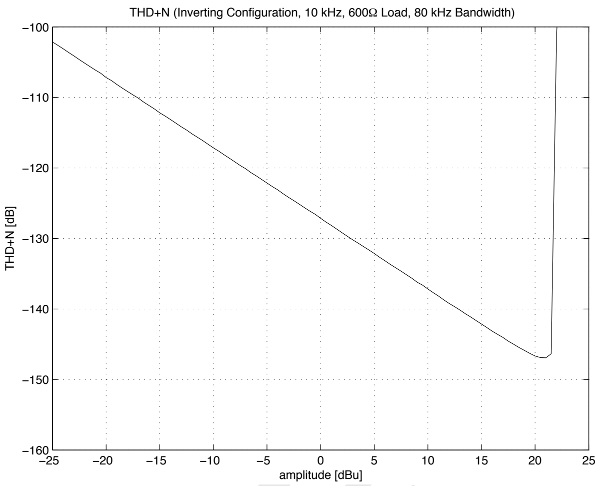

THD+N (Inverting Configuration, 10 Hz, 200Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

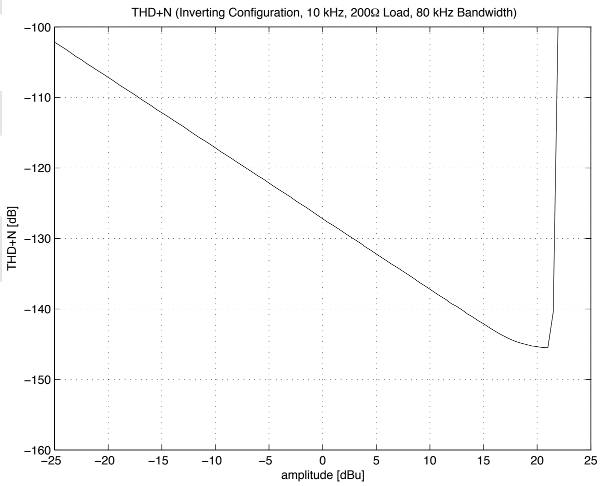

THD+N (Inverting Configuration, 100 Hz, 600Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

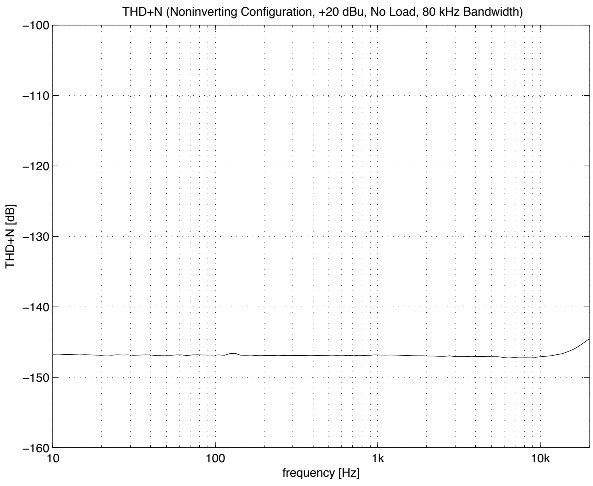

THD+N (Inverting Configuration, 100 Hz, 200Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

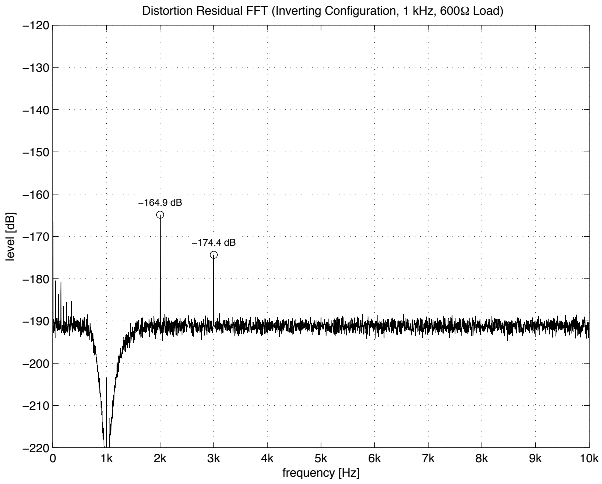

THD+N (Inverting Configuration, 1 kHz, 600Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

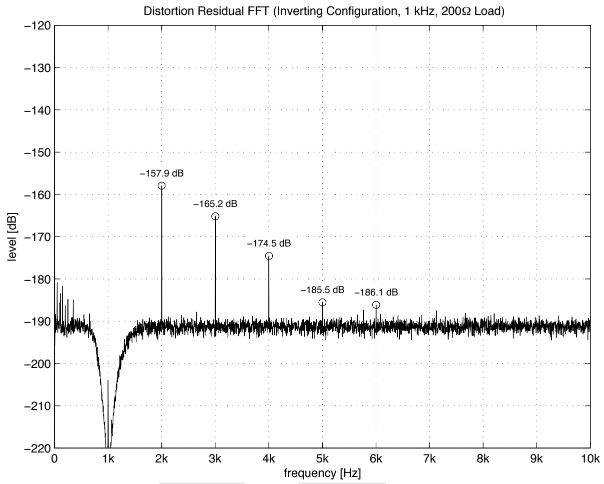

THD+N (Inverting Configuration, 1 kHz, 200Ω Load, 22 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

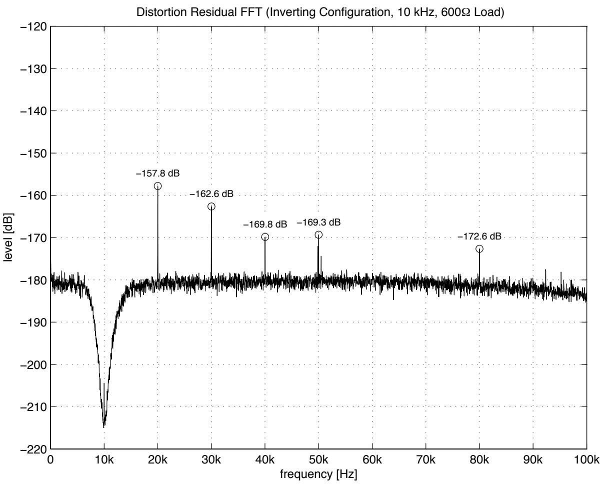

THD+N (Inverting Configuration, 10 kHz, 600Ω Load, 80 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

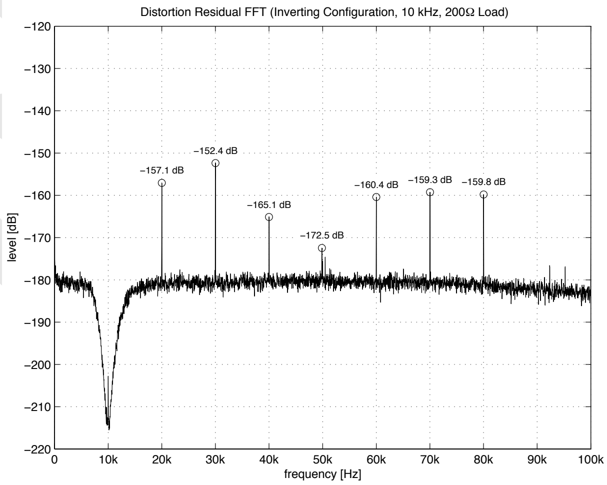

THD+N (Inverting Configuration, 10 kHz, 200Ω Load, 80 kHz Bandwidth)
THD+N [dB]
amplitude [dBu]

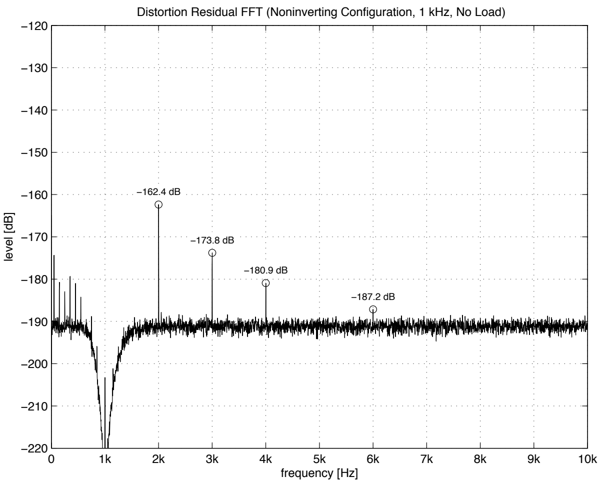

THD+N (Noninverting Configuration, +20 dBu, No Load, 80 kHz Bandwidth)
THD+N [dB]
frequency [Hz]

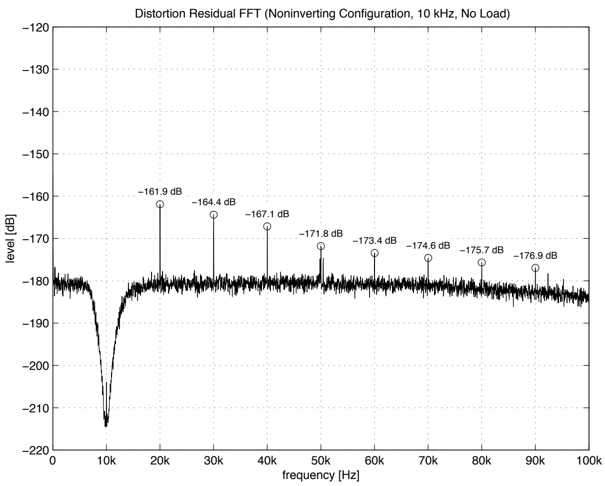

Distortion Residual FFT (Inverting Configuration, 1 kHz, 600Ω Load)
−164.9 dB
−174.4 dB
level [dB]
frequency [Hz]

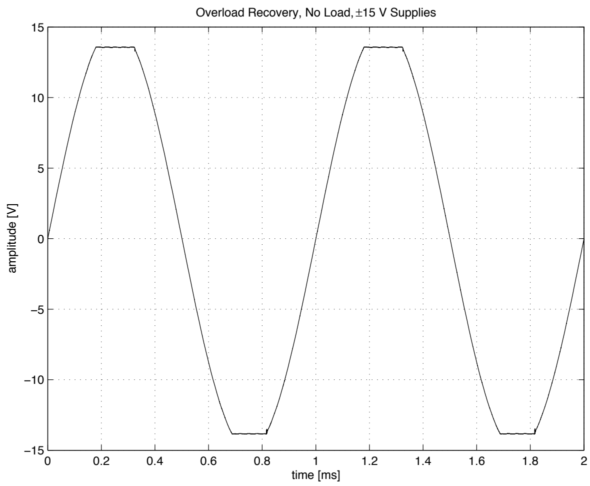

Distortion Residual FFT (Inverting Configuration, 1 kHz, 200Ω Load)
−157.9 dB
−165.2 dB
−174.5 dB
−185.5 dB
−186.1 dB
level [dB]
frequency [Hz]


Distortion Residual FFT (Inverting Configuration, 10 kHz, 600Ω Load)
−157.8 dB
−162.6 dB
−169.8 dB
−169.3 dB
−172.6 dB
level [dB]
frequency [Hz]

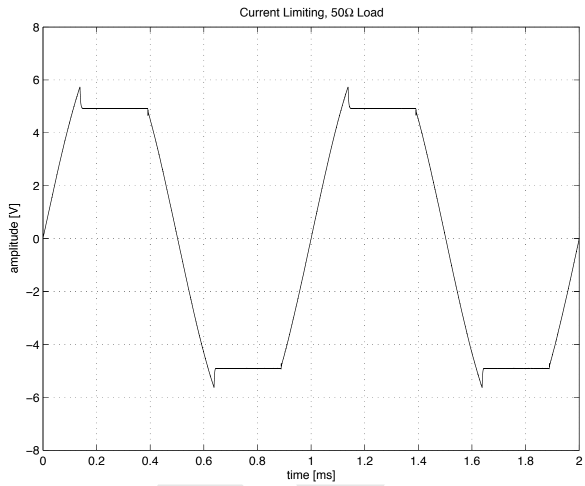

Distortion Residual FFT (Inverting Configuration, 10 kHz, 200Ω Load)
−157.1 dB
−152.4 dB
−165.1 dB
−172.5 dB
−160.4 dB
−159.3 dB
−159.8 dB
level [dB]
frequency [Hz]


Distortion Residual FFT (Noninverting Configuration, 1 kHz, No Load)
−162.4 dB
−173.8 dB
−180.9 dB
−187.2 dB
level [dB]
frequency [Hz]

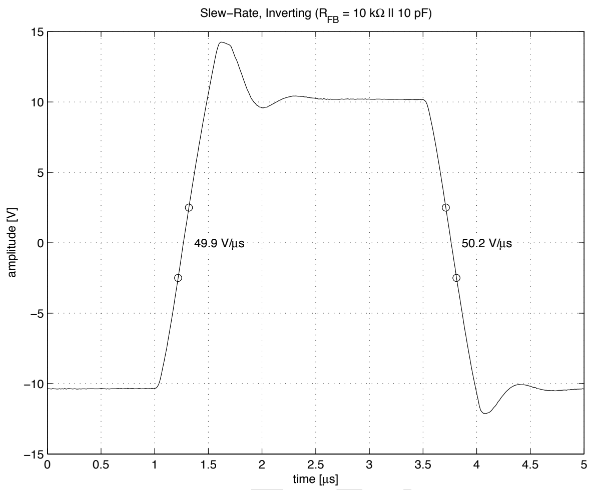

Distortion Residual FFT (Noninverting Configuration, 10 kHz, No Load)
−161.9 dB
−164.4 dB
−167.1 dB
−171.8 dB
−173.4 dB
−174.6 dB
−175.7 dB
−176.9 dB
level [dB]
frequency [Hz]



Overload Recovery, No Load, ±15 V Supplies
amplitude [V]
time [ms]



Current Limiting, 50Ω Load
amplitude [V]
time [ms]



Slew−Rate, Inverting (R FB = 10 kΩ || 10 pF)
49.9 V/µs
50.2 V/µs
amplitude [V]
time [µs]

Chapter 5

Theory Of Operation

5.1 Discrete vs. IC Operational Amplifiers

Operational amplifiers fabricated as integrated circuits (IC) are in ubiquitous use due to their low cost, small size and generally speaking good performance. However discrete amplifier implementation offers substantial advantages if highest performance is in demand; hence this route has been taken for the OP1-BP.

Within an integrated circuit all components are tightly thermally coupled. This results in considerable interaction of the various amplifier stages; particularly troublesome is differential heating of the input stage as a result of output stage power dissipation. This alters open loop gain and causes additional low-frequency and intermodulation distortion. With a discrete implementation input and output stage (as well as any other critical circuitry) can be physically separated by a suitable layout. As thermal coupling then mostly happens through air (which is a weak thermal conductor) thermal effects are most effectively reduced to insignificant levels.

Amplifiers implemented as integrated circuit typically include parasitic semiconductor elements (mostly diodes) which connect to the IC substrate. The associated voltage-dependent junction capacitances can lead to excess high-frequency distortion at critical amplifier nodes. Particularly objectionable is voltage dependent capacitance at the opamp noninverting input; this will lead to very high levels of distortion if the amplifier is used in a noninverting configuration and driven from a high source impedance. Discrete circuits are inherently free from parasitic substrate elements and hence do not suffer from these deficiencies.

The maximum power dissipation of typical IC packages (in particular the more recent SMD types) is very restricted. This limits both quiescent current and maximum output current to values below that required for best distortion performance and load driving capability. The package used for the OP1-BP can dissipate several Watts; this allows optimum definition of bias conditions and enables direct drive of very low impedance loads.

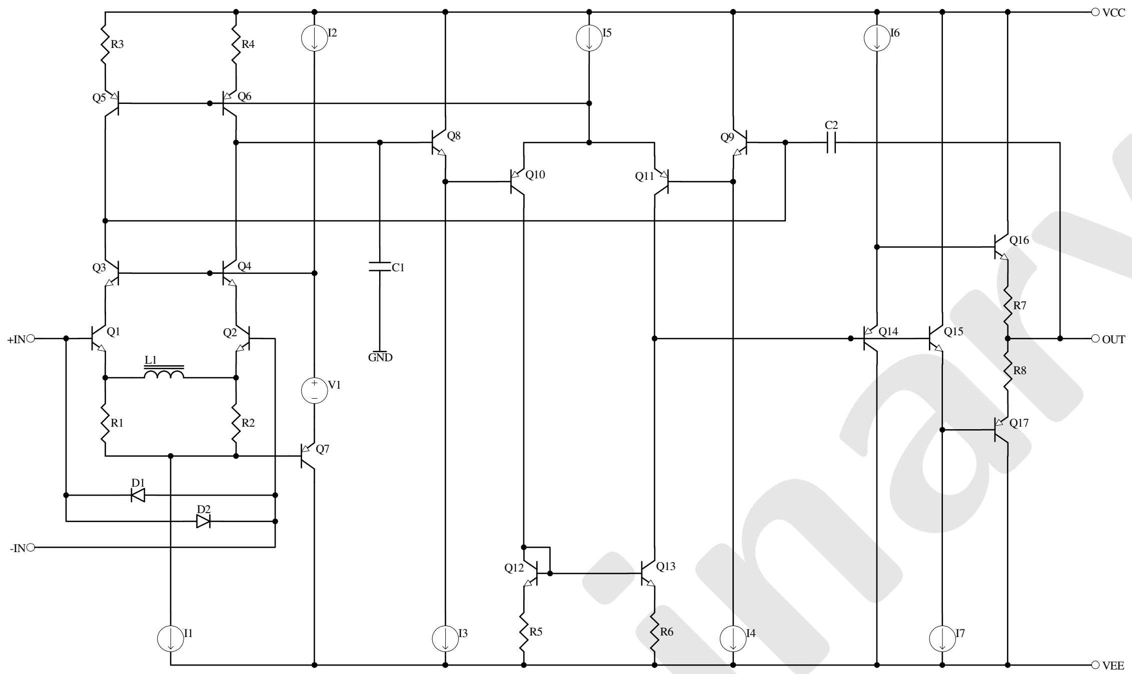


Figure 5.1: OP1-BP simplified schematic.

Inductors of reasonable high value cannot be manufactured with current (and likely any future) IC technology. The use of inductors in the input stage of the OP1-BP however enable a unique combination of high slew-rate and very low noise. This is achieved without use of nonlinear slew-enhancement techniques (such as dynamic input stage current boosting) which typically result in excess high-frequency distortion.

While resistors and capacitors manufactured on IC substrates can be designed to have excellent matching characteristics their absolute tolerance is typically quite poor (10 % or even worse), at least unless trimming techniques are used. Due to the exclusive use of precision resistors, inductors, capacitors and bias voltage reference elements the consistency of the OP1-BP is exemplary. In addition to this discrete passives offer lower noise, lower voltage coefficient and better stability over typical IC implementations.

5.2 Amplifier Architecture and Implementation

The OP1-BP features an architecture and implementation with unique properties resulting in performance far superior to previously available operational amplifiers. Figure 5.1 shows a simplified schematic of the amplifier. The input stage (Q1, Q2) is designed to have frequency-dependent transconductance. At low and medium frequencies (up to about 50 kHz) the transconductance is high because L1 shorts the emitter degeneration resistors R1 and R2. This provides high open loop gain and low voltage noise at these frequencies. At high frequencies (above 50 kHz) the degeneration resistors R1 and R2 become active and reduce the input stage transconductance. This allows the choice of low-value compensation capacitors (C1, C2) for very high slew-rate and excellent large signal bandwidth.

The collectors of the input differential pair (Q1, Q2) are bootstrapped to the common-mode input voltage by means of cascode transistors Q3 and Q4. This benefits both CMRR and PSRR of the amplifier and minimises the thermal dissipation of Q1 and Q2 which in turn lowers voltage noise and sensitivity to thermal gradients. The bootstrapping cascode connection also greatly increases the common-mode input impedance of the amplifier, and reduces the voltage dependence of this parameter. The later is particularly important if the amplifier is used in a noninverting configuration and driven by a high source impedance. Significant voltage dependence of the common-mode input impedance results in considerable distortion as the amplifier input impedance forms a nonlinear voltage divider together with the source impedance. Further improvement of the common-mode performance is achieved by the use of a precision, very high impedance current generator I1 for the input stage.

R3 and R4 are factory trimmed for lowest input offset voltage and drift. Input bias current compensation (not shown in the simplified schematic) is employed to reduce DC errors from bias currents flowing into source and feedback resistors. The conventional bias current compensation schemes typically used in operational amplifiers increase current noise and voltage dependence of the common-mode input impedance. Due to particular attention in the design of the OP1-BP these effects are effectively eliminated.

The second stage (Q8–Q13) features a differential topology. The resulting fully balanced interface to the first stage enables very high CMRR along with high open loop gain and low drift. The Miller compensation with capacitor C2 is carried out with reference to the ground pin (note the ground connection of C1). In other words the output of the amplifier at high frequencies is referenced to the ground potential. For essentially all conventional amplifiers the output at high frequencies is referenced to one supply rail, resulting in poor high frequency power supply rejection. The PSRR of the OP1-BP is largely frequency independent within the audio frequency range. The Miller compensation loop formed by C2 includes the output stage; this reduces output impedance and distortion.

The output stage (Q14–Q17) is a folded darlington type. It combines high output voltage swing with low output impedance, excellent distortion characteristics and good thermal stability. Bias is factory set such that for output currents up to ±30 mA class A operation is ensured; the user can adjust the class A output current to values from about ±10 mA to ±50 mA by means of a trimmer (see section 6.3). The output current limiting circuitry (not shown in the simplified schematic) features output voltage dependent current limiting (i.e. for output voltages near the supply voltage maximum output current is increased). In contrast to the typically used constant current limiting this greatly improves load driving capability and amplifier protection.

Particular attention has been paid to the thermal management of the amplifier. The output stage can dissipate considerable power, which should not affect the operating conditions of the small-signal stages; this has been achieved by thermal isolation of the small-signal stages from the output stage transistors. The biasing circuit of the amplifier is designed to keep performance independent of ambient temperature. In particular slew-rate and output stage quiescent current are kept constant with temperature. Amongst other design techniques this is a result of the extensive use of dual matched transistors which ensure tight tracking of important parameters.

5.3 Manufacturing Information

The manufacturing process of the OP1-BP is targeted for best performance, consistency and reliability. After the four layer printed circuit board is assembled and soldered the output stage heatsink is attached with a high-performance adhesive for a reliable, low loss connection. The fully assembled amplifier circuit is now exposed to several thermal cycles. This burn-in procedure ensures very stable operation afterwards, particularly regarding DC precision and the various bias points. Subsequently offset voltage, input bias current and class A output current are trimmed with the amplifier fully warmed up. Extensive testing of each specimen is carried out for several critical parameters.

Chapter 6

Applications Information

6.1 Noise and Source Impedance Considerations

The very low voltage noise density of $1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{kHz}$ is achieved by the use of input transistors with low base spreading resistance and high collector currents. Unlike typical operational amplifiers the current noise density is simultaneously kept low at $0.7\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ ($1\,\mathrm{kHz}$).[1] For optimum noise performance it is however important to consider the effects of source resistance and amplifier noise current. To calculate the total input-refered voltage noise density three contributions need to be considered:

- Thermal noise density of the source resistance: $\sqrt{4kT \cdot R_S}$
- Voltage noise density of the amplifier: e_N
- Current noise density of the amplifier: $i_N \cdot R_S$

The overall amplifier noise contribution is then given by $\sqrt{e_N^2 + (i_N \cdot R_S)^2}$ and the total noise by $\sqrt{4kT \cdot R_S + e_N^2 + (i_N \cdot R_S)^2}$. These two functions and thermal source resistance noise density are plotted in figure 6.1 and 6.2 for source resistances from $10\,\Omega$ to $100\,\mathrm{k}\Omega$. The graphs are valid for both balanced and unbalanced source resistance configurations as there is no significant common-mode current noise.

It can be seen that opamp voltage noise density dominates for source resistances below $65\,\Omega$ only at both $1\,\mathrm{kHz}$ and $10\,\mathrm{Hz}$. For source resistances above $33\,\mathrm{k}\Omega$ opamp current noise density is the major contribution at $1\,\mathrm{kHz}$; the according source resistance at $10\,\mathrm{Hz}$ is $8.3\,\mathrm{k}\Omega$.

Reactive source impedances (capacitors and inductors) do not have an intrinsic thermal noise contribution. However, the amplifier current noise i_N still contributes to total voltage noise. The OP1-BP is an optimum choice for low

[1] The current noise density of a typical IC amplifier with a voltage noise performance similar to the OP1-BP is around $2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{kHz}$.

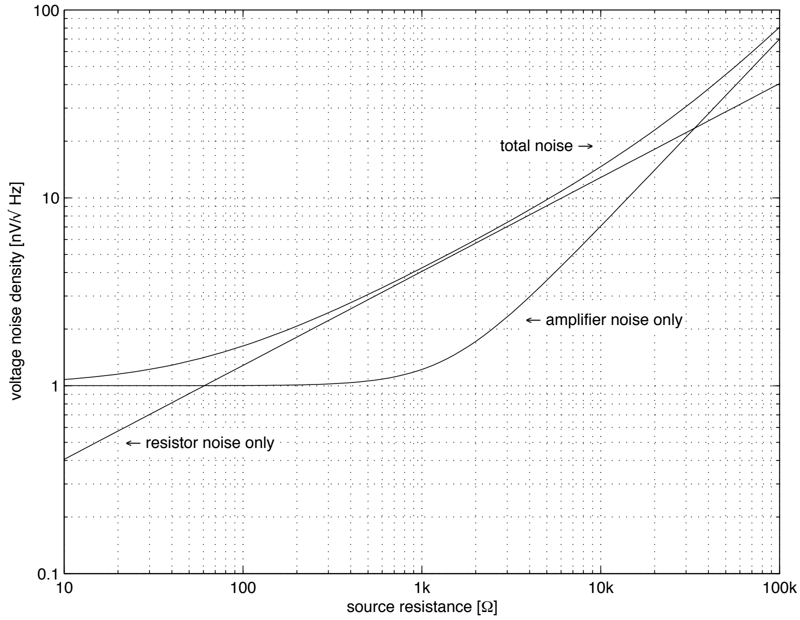


Figure 6.1: Input-refered voltage noise density vs. source resistance at 1 kHz.

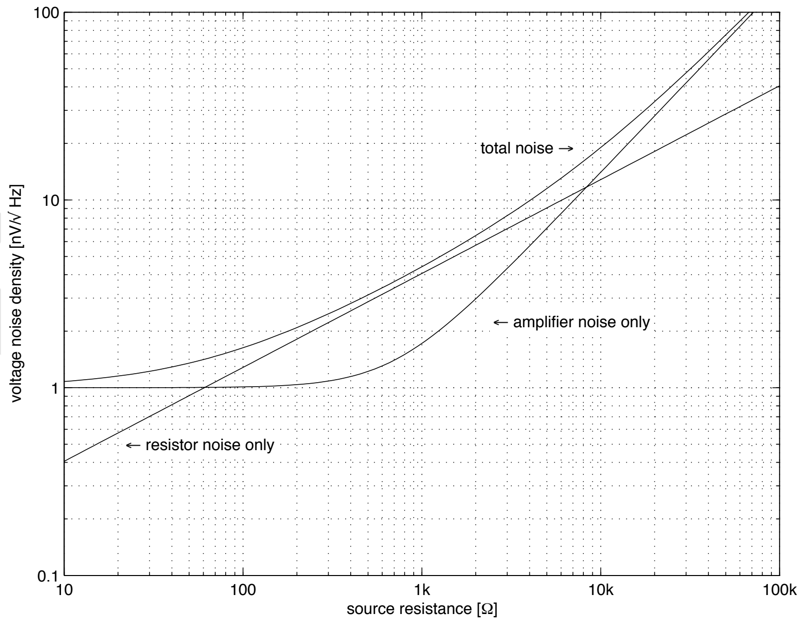


Figure 6.2: Input-refered voltage noise density vs. source resistance at 10 Hz.

noise provided the total source impedance (which includes the feedback network) is kept below about 20 kΩ (at 1 kHz) or 5 kΩ (at 10 Hz).

6.2 Low Distortion Implementation

The OP1-BP is particularly suited for low distortion applications. Unlike typical amplifiers its distortion performance is to a great extent independent of load impedance, source impedance and magnitude of common-mode AC input voltage. Implementations for low distortion often have involved compromises with respect to noise and/or complexity. This is not necessary with the OP1-BP, and high performance signal pathes result even with basic textbook circuits.

For full benefit of the excellent opamp performance attention to the passive components of the feedback network is needed. Low-value feedback resistors can dissipate considerable power (e.g. 0.5 W peak for a 560 Ω resistor at full output swing of ±17 V). To avoid introduction of low-frequency distortion due to the temperature coefficient of these resistors the use of precision resistors with sufficient power rating and low temperature coefficient is necessary. Also of concern is the voltage coefficient of resistors. Metal film and wirewound resistors typically are axcellent with this respect; if in doubt the use of series-connected resistors instead of one single part should be considered to reduce the voltage swing across the resistor.

Capacitors which experience considerable AC voltage swing at frequencies of interest (e.g. in equalising and filtering networks) should have low voltage coefficient. Suitable dielectrica include ceramic C0G/NP0, polypropylene film, polystyrene film and Teflon® film. Again the use of multiple series-connected capacitors instead of a single part may be considered to reduce voltage swing and hence distortion.

Lowest amplifier distortion is achieved for output currents which operate the output stage in class A. Due to the high current gain of the output stage and the inclusive Miller compensation distortion is still notably low in class AB operation; however additional care must be given to the layout as the power supply traces now carry heavily distorted (essentially rectified) signal-dependent AC currents. These can induce into sensitive circuitry and cause distortion if left unchecked. Routing of the power supply traces carrying the distorted AC currents should be spaced away from sensitive (e.g. strongly inductive, high impedance or low level) nodes. Additionally negative and positive supply should be routed in close proximity as their added magnetic fields ideally result in an undistorted replica of the opamp output current.

6.3 Class A Output Current Adjustment

The quiescent current of the output stage can be adjusted by a trimmer; this allows a user-defined trade-off between quiescent power dissipation and maximum class A output current. The typical trimming range for the class A output current is ±10 mA to ±50 mA.

There are two trimmers on the OP1-BP printed circuit board. The one used to set the output stage quiescent current is located close to the power output transistors and not sealed. In the corner of the printed circuit board next to the output stage there are two test points which are used to measure the actual quiescent current. To achieve a class A peak output current I_{OUT} the DC voltage across the two test points[2] V_Q must be set as follows:

$$V_Q = 4.1\,\Omega \cdot I_{OUT} + 7\,\text{mV} \qquad (6.1)$$

During the measurement it is recommended that the operational amplifier is operated with zero output current and fully warmed up. Also the class A output current shows a slight dependence on power supply voltage; typically it decreases by about 18 % when going from ±5 V to ±18 V power supplies. Hence adjustment should be done at the correct power supply voltage.

The operational amplifiers are factory preset to a class A peak output current of ±30 mA with ±15 V power supplies; this value will be sufficient for full class A operation in most cases.

6.4 DC Precision

There are three amplifier parameters which influence its DC precision at a given temperature: offset voltage, input bias current and input offset current. The offset voltage of the OP1-BP is trimmed to a very low value of typically ±10 μV with the amplifier fully warmed up. As the offset and drift contribution of the second amplifier stage have been kept low zeroing the amplifier offset voltage will also lead to very low offset voltage drift. As there is hence no need for further offst voltage trimming the according trimmer is sealed after adjustment to prevent inadverted readjustment.

For configurations where the input terminals of the amplifier see a source resistance unbalance of more than 170 Ω input bias current will typically dominate DC precision. It is hence possible to further increase the DC precision by external input bias current cancellation. Figure 6.3 displays the suggested implementation for a noninverting amplifier (typically $R_S \gg R_1 \parallel R_2$) configuration; other amplifier configurations may use a similar bias cancellation scheme. To approximately track the temperature coefficient of the input bias current the cancellation current is derived from forward biased diodes. This also ensures low noise contribution.

The input bias current cancellation scheme of the OP1-BP has been designed to contribute little to input offset current; only with well balanced source

[2] The two test points are isolated by resistors, so accidentally shorting the test points will not damage the amplifier.

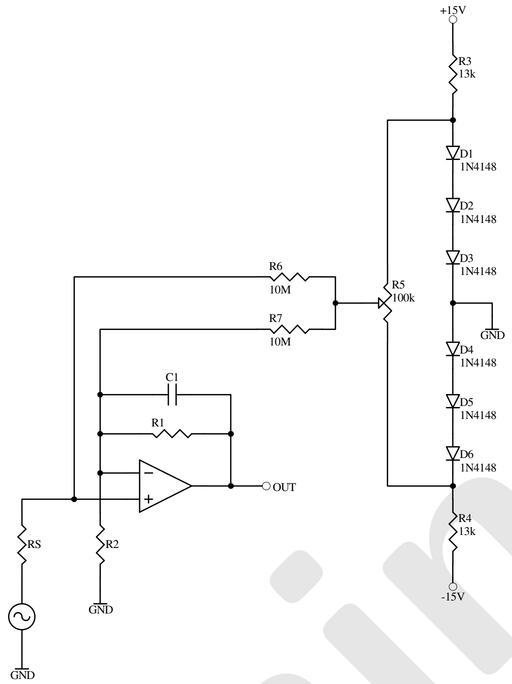


Figure 6.3: Input bias current cancellation.

resistances above 5 kΩ will the amplifier offset current dominate DC precision. In such cases the cancellation scheme of figure 6.4 may be used. Again the reference voltage is derived from forward biased diodes for low noise and suitable temperature coefficient. Shown is a differential amplifier configuration ($R_1 = R_2$ and $R_3 = R_4$), but a similar offset current cancellation scheme may be used for other amplifier configurations with matched source resistances at the input terminals.

6.5 Ground Pin Connection

The ground pin of the amplifier should be connected to a signal ground point with low high-frequency impedance; for proper operation the ground potential should be approximately in between the two supply rails, and needs to be able to supply a DC current of 10 μA. Operation with ground potentials as close as 2 V to the supply rails is possible but not recommended as it might adversely affect the internal thermal balance of the amplifier circuit.

6.6 Feedback Capacitor Selection

Due to the frequency-dependent gain bandwith product of the OP1-BP simple resistive feedback results in gain peaking and overshoot. This is easily avoided

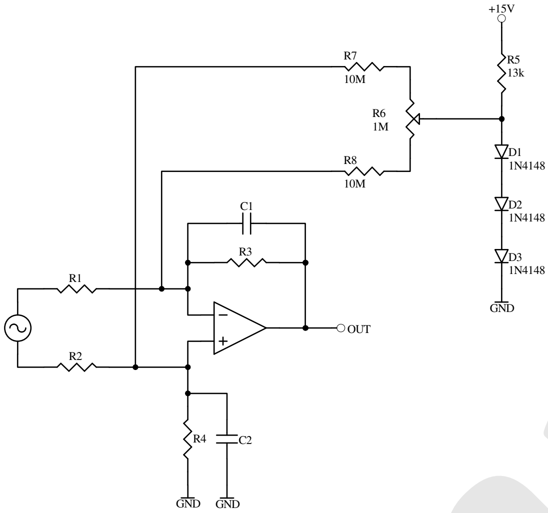


Figure 6.4: Input offset current cancellation.

by the use of a suitable feedback capacitor. Figure 6.5 shows recommended minimum time constant values t for the RC feedback network. For a given feedback resistor value R_{FB} the minimum feedback capacitor value C_{FB} can be estimated as follows:

$$C_{FB} = \frac{t}{2\pi \cdot R_{FB}}$$

If overshoot-free transient response is not necessary, the capacitor values can be chosen about 30 % lower for maximum bandwidth. This will still avoid gain peaking.

In any case the time constant as shown in figure 6.5 should be considered an initial estimate only. Details of the exact implementation (e.g. feedback network impedance and layout stray capacitances) may affect the required feedback capacitor value and experimental verification is needed.

6.7 Power Supply Bypassing and Layout Considerations

The OP1-BP includes a total of 2.4 μF of high quality, low impedance on-board decoupling capacitors. Together with the excellent power supply rejection of the amplifier this is in essentially all cases sufficient for stability and no external high-frequency bypassing is needed. With long power supply traces and low impedance loads it is nonetheless advisable to arrange for electrolytic bypass capacitors from the supply rails to load ground. Recommended values range from 47 μF to 220 μF.

For best performance and stable operation care to layout is needed. It is recommended to place the feeback network below the amplifier for short traces

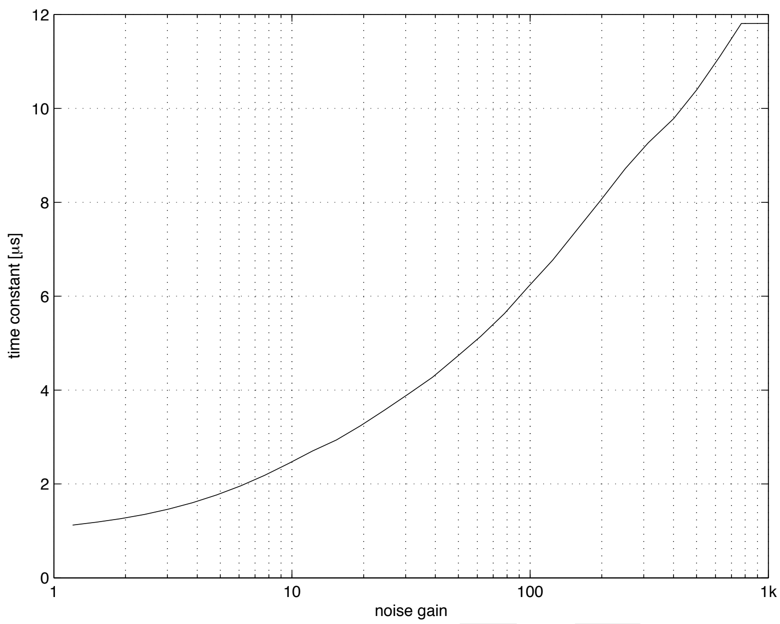


Figure 6.5: Minimum time constant of RC feedback network vs. noise gain for overshoot-free transient response.

and minimum layout parasitics (particularly stray capacitance at the inverting input). Ground planes should be used.

6.8 Driving Capacitive Loads

Due to its output stage with very low output impedance the OP1-BP is able to drive high capacitive loads directly, typically up to 1 nF. Higher or unknown capacitive loads (e.g. cables) should be isolated by a small resistor in series with the amplifier output. To be effective the feedback point must be taken *before* the isolation resistor. A value of 30 Ω for the isolation resistor will in most cases enable unlimited capacitive drive, however experimental verification is suggested and lower values might be suitable for certain conditions (e.g. if the capacitive load is limited to a known maximum value). If low output impedance at low frequencies is required the isolation resistor may be paralleled by an inductor. For low distortion this inductor should be air cored only; as initial value for experimental verification 3 μH or higher is recommended.

6.9 Sockets and Handling

It is recommended to use sockets for the OP1-BP instead of direct soldering to the printed circuit board. Suitable sockets are available from Mill-Max as part no. 0344-2-19-15-34-27-10-0; other manufacturers offer compatible parts.

When handling the amplifiers, particularly during insertion into the sockets, care should be applied in order to not bend or otherwise damage any amplifier part. It is recommended to hold the amplifier at the printed circuit board only; in particular any stress to the power output transistors, heatsink and trimmers should be avoided.

Chapter 7

Outline Dimensions and Pinout